HISTOGRAM PERFORMANCE COUNTERS FOR USE IN TRANSACTION LATENCY ANALYSIS

ABSTRACT OF THE DISCLOSURE

Methods and apparatus are described for measuring latency in computer systems. A computer system includes a processor, memory, and I/O. The processor is operable to initiate transactions involving the memory and the I/O. The computer system further includes a latency counter operable to measure a latency for each of selected ones of the transactions. The system also includes a plurality of histogram counters. Each histogram counter is operable to count the latencies corresponding to an associated latency range.